WHAT IS CLAIMED IS:

1. A ferroelectric memory device comprising:

a plurality of bit line pairs each of which is composed of first and second bit lines;

a plurality of sense amplifiers each for amplifying a potential difference across the corresponding bit line pair;

a plurality of memory cells provided for the bit line pairs, respectively, each of the memory cells being composed of a first ferroelectric capacitor for retaining data and a transistor whose source is connected to a first electrode of the first ferroelectric capacitor and whose drain is connected to the first bit line;

a plurality of reference cells provided for the bit line pairs, respectively, each of the reference cells being composed of a second ferroelectric capacitor for retaining data and a transistor whose source is connected to a first electrode of the second ferroelectric capacitor and whose drain is connected to the second bit line;

a word line connecting gates of the transistors of the memory cells;

a reference word line connecting gates of the transistors of the reference cells;

a cell plate line connecting second electrodes of the ferroelectric capacitors of the memory cells;

a reference cell plate line connecting second electrodes of the ferroelectric capacitors of the reference cells; and

a control circuit for controlling operations of the memory cells, the reference cells, and the sense amplifiers,

wherein the control circuit inactivates the reference word line during the drive of the sense amplifiers.

2. The device of claim 1, further comprising a switch circuit connecting the second bit lines included in adjacent bit line pairs of the plurality of bit line pairs,

wherein the control circuit stops the drive of the switch circuit during the drive of the sense amplifiers.

3. The device of claim 2, wherein the control circuit performs successive actions of:

driving the switch circuit and activating the word line, the cell plate line, the reference word line and the reference cell plate line;

inactivating the cell plate line and the reference cell plate line;

inactivating the reference word line;

stopping the drive of the switch circuit; and

driving the sense amplifiers.

4. The device of claim 2, wherein the control circuit performs successive actions of:

driving the switch circuit and activating the word line, the cell plate line, the reference word line and the reference cell plate line;

inactivating the cell plate line and the reference cell plate line;

stopping the drive of the switch circuit;

inactivating the reference word line; and

driving the sense amplifiers.

5. The device of claim 2, wherein the control circuit performs successive actions of:

driving the switch circuit and activating the word line, the cell plate line, the reference word line and the reference cell plate line;

inactivating the reference word line;

stopping the drive of the switch circuit;

inactivating the cell plate line and the reference cell plate line; and

driving the sense amplifiers.

6. The device of claim 2, wherein the control circuit performs successive actions of:

driving the switch circuit and activating the word line, the cell plate line, the reference word line and the reference cell plate line;

stopping the drive of the switch circuit;

inactivating the reference word line;

inactivating the cell plate line and the reference cell plate line; and

driving the sense amplifiers.

7. The device of claim 2, wherein the control circuit performs successive actions of:

driving the switch circuit; and

activating the word line, the cell plate line, the reference word line and the reference cell plate line.

8. The device of claim 2, wherein the control circuit performs successive actions of:

activating the reference word line and the reference cell plate line for a predetermined period of time;

driving the switch circuit for a predetermined period of time; and

driving the sense amplifiers.

9. A method for reading data from a ferroelectric memory device,

wherein the ferroelectric memory device includes: a plurality of bit line pairs each of which is composed of first and second bit lines; a plurality of sense amplifiers each for amplifying a potential difference across the corresponding bit line pair; a plurality of memory cells provided for the bit line pairs, respectively, each of the memory cells being composed of a first ferroelectric capacitor for retaining data and a transistor whose source is connected to a first electrode of the first ferroelectric capacitor and whose drain is connected to the first bit line; a plurality of reference cells provided for the bit line pairs, respectively, each of the reference cells being composed of a second ferroelectric capacitor for retaining data and a transistor whose source is connected to a first electrode of the second ferroelectric capacitor and whose drain is connected to the second bit line; a word line connecting gates of the transistors of the memory cells; a reference word line connecting gates of the transistors of the reference cells; a cell plate line connecting second electrodes of the ferroelectric capacitors of the memory cells; a reference cell plate line connecting second electrodes of the ferroelectric capacitors of the reference cells; a control circuit for controlling operations of the memory cells, the reference cells, and the sense amplifiers; and a switch circuit connecting the second bit lines included in adjacent bit line

pairs of the plurality of bit line pairs,

the method comprising:

a first step of activating the word line and the reference word line;

a second step of activating the cell plate line and the reference cell plate line for a predetermined period of time;

a third step of activating a switch control signal for driving the switch circuit;

a fourth step of inactivating the reference word line after the first step;

a fifth step of inactivating the switch control signal after the third step; and

a sixth step of driving the sense amplifier for a predetermined period of time after the fourth step.

10. The method of claim 9, wherein the sixth step is performed after the fifth step.

11. The method of claim 9, wherein the fifth step is performed after the fourth step.

12. The method of claim 9, wherein the fifth step is performed before the fourth step.

13. The method of claim 9, wherein the second step is kept on until after the initiation of the sixth step.

14. The method of claim 9, wherein the first step is performed after the third step.

15. The method of claim 9, wherein the third step is performed after the fourth step.